WHAT IS CLAIMED IS:

1. A data communication interface operable to communicate with a device, comprising:

bus circuitry for transferring data;

storage circuitry coupled to the device and to said bus;

interface circuitry operable to shift data between said bus and said storage circuitry; and

device access control circuitry operable to transfer data between said device and said storage circuitry responsive to a control signal.

2. The data communication interface of Claim 1 wherein said device comprises a memory.

3. The data communication interface of Claim 1 wherein said storage circuitry comprises a register.

4. The data communication interface of Claim 3 wherein said storage circuitry comprises a shift register.

5. The data communication interface of Claim 4 wherein said interface circuitry is operable to shift data from said bus circuitry to said shift register and from said shift register to said bus circuitry.

6. The data communication interface of Claim 5 and further comprising a plurality of shift registers coupled to said bus circuitry.

7. The data communication interface of Claim 6 wherein said interface circuitry is operable to shift

data between said bus circuitry and a selected one of said shift registers.

8. The data communication interface of Claim 1 wherein said device access control is operable to transfer data between said device and said storage circuitry responsive to a signal from said interface circuitry.

9. The data communication interface of Claim 8 wherein said device access control is operable to transfer data between said device and said storage circuitry responsive to a pause signal from said interface circuitry.

10. The data communication interface of Claim 1 wherein said device access control is operable to transfer data between said device and said storage circuitry responsive to receiving a predetermined sequence of data.

11. The data communication interface of Claim 10 wherein said device access control includes:

a first register for receiving and storing data;

a second register for storing said predetermined sequence of data; and

compare circuitry for generating a signal responsive to a match between the data stored in said first and second registers.

12. The data communication interface of Claim 1 wherein said device access control is operable to transfer data between said device and said storage circuitry responsive to signal indicating that a counter has counted to a predetermined number.

13. The data communication interface of Claim 12 wherein said device access controller includes:

a counter coupled to said bus circuitry and operable to increment a value stored therein responsive to a clocking signal;

circuitry to output a control signal responsive to said counter storing a predetermined value.

14. The data communication interface of Claim 12 wherein said device access controller includes:

a counter coupled to said bus circuitry and operable to decrement a value stored therein responsive to a clocking signal;

circuitry to output a control signal responsive to said counter storing a predetermined value.

15. The data communication interface of Claim 1 and further comprising a bus controller coupled to said bus and operable transmit data thereon.

16. The data communication interface of Claim 15 wherein said bus controller is further operable to receive data from said bus.

17. A data communication interface operable to communicate with a device, comprising:

bus circuitry for transferring data;

storage circuitry coupled to said bus circuitry and operable to selectivley shift data in from said bus circuitry and shift data out to said bus circuitry;

device interface circuitry operable to control data transfer between said bus circuitry and said storage circuitry; and

device access control circuitry operable to control data transfer between said bus circuitry and said storage circuitry such that data can be written to or read from the device without the need to repetitively cycle through multiple shift operations.

18. The data communication interface of Claim 17 wherein said device access control circuitry is operable to write data to the device responsive to one or more control signal.

19. The data communication interface of Claim 18 wherein said one of said control signals is generated by said device interface circuitry.

20. The data communication interface of Claim 19 wherein said device interface circuitry comprises a state machine and one or more of said control signals are associated with predetermined states of the state machine.

21. The data communication interface of Claim 20 wherein one of said predetermined states is a pause state.

22. The data communication interface of Claim 18 wherein one of said control signals is generated responsive to the recognition of a predetermined sequence of data.

23. The data communication interface of Claim 18 wherein said device access control circuitry includes a counter, one of said control signal generated responsive to a count of a predetermined value.

24. The data communication interface of Claim 18 wherein one of said control signal is received from an external device.

25. A method of communicating with a device coupled to a target interface circuit associated with a serial data bus coupled to a plurality of interface circuits, comprising the steps of:

transferring data from the device into a register associated with the target interface circuit;

shifting data from the register onto the bus;

transferring additional data from the device into the register after the last data bit is shifted out of the register.

26. The method of Claim 25 wherein said step of shifting data from the register comprises the step of shifting data sequentially through ones of said interface circuits.

27. The method of Claim 26 and further comprising the step of counting the number of data bits transferred from the register.

28. The method of Claim 26 and further comprising the step of generating a control signal indicating that the data stored in the register has been transferred to the bus.

29. The method of Claim 25 and further comprising the steps of:

shifting data onto the bus and sequentially through each interface circuit preceding the target interface circuit;

generating a control signal indicative of said data shifted onto the bus reaching said target interface circuit; and

transferring data from a register associated with said target interface circuit to said device responsive to said control signal.

30. A method of communicating with a device coupled to a target interface circuit associated with serial data bus circuitry coupled to a plurality of interface circuits, comprising the steps of:

shifting data onto the bus and sequentially through each interface circuit preceding the target interface circuit;

generating a control signal indicative of data reaching said target interface circuit; and

transferring data from a register associated with said target interface circuit to said device responsive to said control signal.

31. The method of Claim 30 and further comprising the step of loading registers associated with the interface circuits preceding the target interface circuit with a predetermined value.

32. The method of Claim 30 and further comprising the step of loading the register associated with the target interface circuit under control of a device interface circuit.

33. The method of Claim 32 wherein said generating step comprises the step of generating the control signal responsive to a state of said device interface circuit.

34. The method of Claim 30 wherein said generating step comprises the step of generating the control signal responsive to recognition of a predetermined sequence of data.

35. The method of Claim 30 wherein said generating step comprises the step of generating the control signal responsive to a count of a predetermined value.

36. The method of Claim 30 wherein said generating step comprises the step of generating the control signal responsive to a control signal generated by a circuit external to the target interface circuit.